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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,844	12/31/2001	Paras Shah	200302053-1	9675

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EXAMINER	
KING, JUSTIN	
ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/038,844	SHAH ET AL.	
	Examiner	Art Unit	
	Justin I. King	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *11/10/05*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 15 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. The claim 15 recites that one of the grandchild links is associated with a transaction identifier; which does not further limit the claim 12, which recites that a transaction identifier is associated with one grandchild link.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-16, 18-24, 26-28, and 39-40 are rejected under 35 U.S.C. 102(b) as being anticipated by Hausauer (U.S. Patent No. 6,138,192)

Referring to claim 1: Hausauer discloses a three-level PCI bridge architecture with a child link (figure 1, link between structures 18 and 20), and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link, and each PCI transaction ID is the transaction identifier. Hausauer discloses devices (figure 1, structure

32) attached to the grandchild link (figure 1, structure 30); thus, the communication between the devices attached to the grandchild link and the CPU is the claimed transactions associated with a respective grandchild-link. Hausauer further discloses a plurality of transaction order queues (column 4, lines 29-31). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Since the communication between the CPU and the devices attached to the grandchild link must go through the child link (figure 1, structure 19), Hausauer discloses transactions order queues receiving the plurality of transaction from the child link; and since Hausauer discloses that each pair of communicating devices only uses one particular buffer/queue block, Hausauer discloses that the transactions identifier associated with the transaction is uniquely associated with only one of the plurality of transaction order queues and is associated with one of the grandchild links. Hence, claim is anticipated by Hausauer.

Referring to claim 2: Hausauer's transaction identifier communication link comprises the child link.

Referring to claim 3: Hausauer discloses the transaction buffer (figure 5).

Referring to claim 4: Hausauer discloses a plurality of buffers (column 4, lines 29-31).

Referring to claim 5: Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting; each of Hausauer's transaction buffer sets is a channel. Since each transaction has a unique transaction identifier, Hausauer's channels receive the plurality of transaction identifiers.

Referring to claim 6: Hausauer discloses a plurality of child links (figure 1, connections between structure 20 and structures 22, 24, and 26). As stated above, Hausauer discloses sets of

buffers/queue blocks for each PCI device pair transacting via the bridge; thus, Hausauer discloses a plurality of transaction order queues associated with each of the plurality of child links.

Referring to claim 7: Hausauer discloses that the transaction order queues can be either permanently or dynamically assigned to one particular PCI slot (Column 4, lines 39-41). Hence, when the transaction order queue is permanently assigned to one particular PCI slot, the means to direct the transactions from the particular PCI slot to the assigned transaction order queue is the claimed routing mechanism.

Referring to claim 8: As stated above, Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge, and each transaction has a unique transaction identifier; thus, Hausauer's transaction order queue is associated with a transaction order queue identifier uniquely matching a transaction identifier.

Referring to claim 9: Hausauer discloses that the transaction order queues can be either permanently or dynamically assigned to one particular PCI slot (Column 4, lines 39-41). Hence, when the transaction order queue is dynamically assigned, the means to assign the transaction order queue is equivalent to the claimed routing a transaction with a transaction identifier without a matching transaction order queue to a default transaction order queue.

Referring to claim 10: Hausauer discloses that the child-link (figure 1, structure 19) connects to a bus-bridge (figure 1, structures 20 and 28).

Referring to claim 11: Hausauer discloses that the child-link (figure 1, structure 19) connects to a bridge-bridge (figure 1, structures 20 and 28).

Referring to claims 12 and 15: Hausauer discloses a three-level PCI bridge architecture with a child link (figure 1, link between structures 18 and 20), and each PCI transaction ID is the transaction identifier. Hausauer discloses a plurality of grandchild-links (figure 1, connections between structure 20 and structures 22, 24, and 26) for receiving a plurality of transactions, and a child link (figure 1, connection between structures 18 and 20) for sending the plurality of transactions; and Hausauer's physical wire to establish the child link (the PCI connections) is the transaction identifier communication link. Since the communication between the CPU and the devices attached to the grandchild link must go through the child link (figure 1, structure 15), Hausauer discloses transactions order queues receiving the plurality of transaction from the child link; and since Hausauer discloses that each pair of communicating devices only uses one particular buffer/queue block, Hausauer discloses that the transactions identifier associated with the transaction is uniquely associated with only one of the plurality of transaction order queues and is associated with one of the grandchild links. Hence, claim is anticipated by Hausauer.

Referring to claim 13: Hausauer discloses a communication link comprises the child link (figure 1, structure 15).

Referring to claim 14: Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting; each of Hausauer's transaction buffer sets is a channel. Since each transaction has a unique transaction identifier, Hausauer's channels receive the plurality of transaction identifiers.

Referring to claim 16: Since each transaction has a unique transaction identifier, and Hausauer discloses two separate grandchild links (figure 1, connections between structures 20 and 22, and between structures 20 and 24), the communications from these two separate

grandchild links discloses at least two grandchild links associated with at least two different transaction identifiers.

Referring to claim 18: Hausauer discloses that the grandchild link is connected to a bus (figure 1, structure 19).

Referring to claim 19: Hausauer discloses that the grandchild link is connected to a bus bridge (figure 1, structures 20 and 28).

Referring to claim 20: Hausauer discloses that the grandchild link is connected to a bridge-bridge (figure 1, structure 20).

Referring to claim 21: Hausauer discloses a three-level PCI bridge architecture with a child link (figure 1, link between structure 19), and each PCI transaction ID is the transaction identifier. Hausauer discloses devices (figure 1, structure 32) attached to the grandchild link (figure 1, structure 30); and since the communication between the CPU and the devices attached to the grandchild link must go through the child link (figure 1, structure 19), the communication between the devices attached to the grandchild link and the CPU is the claimed transaction associated with a respective grandchild link, and the associated transaction identifier for the communication between the devices attached to the grandchild link and the CPU is the claimed indication of the association of the transaction and the respective grandchild link.

Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Hausauer further discloses that the transaction order queues can be either permanently or dynamically assigned to one particular PCI slot (Column 4, lines 39-41). Hence, when the transaction order queue is permanently assigned, the means to route the transaction

order queue is equivalent to the claimed matching the transaction identifier to a transaction order queue such that the associated grandchild links are also uniquely associated with one transaction order queue. Therefore, claim is anticipated by Hausauer.

Referring to claim 22: Hausauer discloses transaction buffers (column 4, lines 28-29) for storing transaction.

Referring to claim 23: As stated above, Hausauer discloses that the transaction order queues can be either permanently or dynamically assigned to one particular PCI slot (Column 4, lines 39-41). Hence, when the transaction order queue is permanently assigned, the means for forwarding transactions to the assigned transaction order queue is equivalent to the claimed matching, routing, and storing transaction identifier to a transaction buffer.

Referring to claim 24: Hausauer discloses the child link (figure 1, structure 19) receiving the transaction.

Referring to claim 26: Hausauer discloses a three-level PCI bridge architecture with a child link (figure 1, link between structure 19), and each PCI transaction ID is the transaction identifier. Hausauer discloses devices (figure 1, structure 32) attached to the grandchild link (figure 1, structure 30); and since the communication between the CPU and the devices attached to the grandchild link must go through both the child link (figure 1, structure 19) and the grandchild link (figure 1, structure 30), Hausauer discloses receiving a transaction on the child link wherein the transaction is associated with a respective grandchild link. And since the transaction identifier is unique, Hausauer's communication between the CPU and the devices attached to the grand link discloses receiving a transaction identifier for the transaction link, wherein the transaction identifier is indicative of the association of the transaction and the

respective grandchild link. Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Therefore, claim is anticipated by Hausauer.

Referring to claim 27: Hausauer's communication between the CPU and the devices attached to the grand link discloses sending identifier to the parent bridge (figure 1, structure 20) on a child link (figure 1, structure 19).

Referring to claim 28: Since each transaction identifier is unique, the transaction identifier is generated and determined by initiating the communication from the grandchild link on which the transaction was received.

Referring to claim 39: Hausauer discloses a three-level PCI bridge architecture with a child link (figure 1, link between structure 19), and each PCI transaction ID is the transaction identifier. Hausauer discloses a plurality of buses (figure 1, structures 14, 15, 19, and 30), a child bridge (figure 1, structure 28) coupled to one bus (figure 1, structures 19 or 30), and a parent bridge (figure 1, structure 20) coupled to the child bridge, wherein the parent bridge includes a plurality of transaction order queue sets (column 4, lines 30-63). Since each queue stores the transaction related data, each queue is corresponding to at least one of the plurality of buses such parent bridge can maintain the information of the transaction between the bus and the transaction. Hausauer's bridge is a PCI bridge; the incorporated PCI bridge specification discloses that it is known to construct a system with multiple child bridge. Hence, the claim is anticipated by Hausauer.

Referring to claim 40: Since each transaction identifier is unique, the transaction identifier for the transaction between the CPU and the device attached to the grandchild link is uniquely associated with only one of the grandchild-links.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 31-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the Hausauer and an Official Notice.

Referring to claim 31: Hausauer discloses a processor (figure 1, structure CPU), a parent bridge (figure 1, structure 20) comprising a child link (figure 1, structure 19) and a plurality of transaction order queues (column 4, lines 29-30), and a child bridge (figure 1, structure 28) connected to the parent bridge via the child link and grandchild link (figure 1, structure 30). Hausauer discloses sets of buffers/queue blocks for each PCI device pair transacting via the

bridge and each pair of PCI devices only uses one particular buffer/queue block (column 4, lines 30-42). Therefore, when the device attached to the grandchild link communicates with CPU, the transaction order queue will store and associate with one grandchild link to provide a one-to-one correspondence between the transaction order queue and grandchild link. Hausauer discloses a PCI bridge; the PCI bridge specification discloses that it is known to equipment a system with multiple grandchild links. Hausauer doesn't disclose multiple processors. An Official Notice is taken as the following: multi-processor system is a well-known practice in the computer art. Hence, it would have been obvious to one having ordinary skill in the computer art to adapt multiple processors into Hausauer because it increases the system performance.

Referring to claim 32: The PCI bridge specification discloses a plurality of child links and child bridges.

Referring to claim 33: Since each transaction has a unique transaction identifier, the communication between the child bridge and parent bridge includes transmitting a transaction and transaction identifier.

Referring to claim 34: Since each transaction's transaction identifier is unique, and Hausauer discloses each pair of communicating devices only uses one particular buffer/queue block (column 4, lines 30-42), Hausauer discloses that each transaction identifier is associated with a transaction order queue.

Referring to claim 35: Since each transaction's transaction identifier is unique, thus, the transaction identifier for the communication between the grandchild link to the CPU exclusively identifies a grandchild link.

Referring to claim 36: Hausauer discloses that the transaction order queues can be either permanently or dynamically assigned to one particular PCI slot (Column 4, lines 39-41). Hence, when the transaction order queue is dynamically assigned, the means to assign the transaction order queue is equivalent to the claimed routing a transaction with a transaction identifier without a matching transaction order queue to a default transaction order queue.

Referring to claims 37-38: Hausauer discloses buffers (column 4, lines 28-62) connected to the child links.

Response to Arguments

7. In response to Applicant's argument that the prior arts on record do not disclose or teach the amended limitations (Remark, page 16): See the revised rejection above. In addition, an interview on confirms that the amended limitations are not necessarily limited to the one-to-one relationship as discussed in the interview dated 9/22/05; the amended limitations do not preclude one-to-many relationship.

Conclusion

8. The prior arts made of recorded from previous Office Action and not relied upon are considered pertinent to applicant's disclosure.

"PCI-X Addendum to the PCI Local Bus Specification" by PCI Special Interest Group, 1999, Rev. 1.0: The Specification discloses the sequence ID for each transaction (page 39, paragraphs 1-2).

"PCI-to-PCI Bridge Architecture Specification" by PCI Special Interest Group, 1998, Rev. 1.1: The Specification discloses the three-tier bridge architectures.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin I. King whose telephone number is 571-272-3628. The examiner can normally be reached on Monday through Friday, 9:00 am to 5:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676 or on the central telephone number, (571) 272-2100. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lastly, paper copies of cited U.S. patents and U.S. patent application publications will cease to be mailed to applicants with Office actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with office actions. These cited U.S. patents and patent application publications are available for download via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), from the Office of Public Records and from

commercial sources. Applicants are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted.

Justin King
November 10, 2005

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
11/14/05